What is claimed is:

1. An apparatus, comprising:

a first memory bank;

a second memory bank capable of having an operational state and a low power state;

a memory controller coupled to the first and second memory banks and comprising a comparator to determine if a current address location in the first memory bank is within a predefined number of address locations from an address location in the second memory bank; and

a memory power controller coupled to the second memory bank to change the second memory bank from the low power state to the operational state resultant to the comparator determining that the current address location is within the predefined number of address locations.

2. The apparatus of claim 1, wherein the low power state is a data-retaining state.

3. The apparatus of claim 1, wherein the second memory bank comprises volatile memory.

4. The apparatus of claim 3, wherein the volatile memory comprises static random access memory.

5. The apparatus of claim 1, further comprising a circuit to place the second memory bank in the low power state resultant to the second memory bank not being accessed within a predetermined interval.

6. The apparatus of claim 5, further comprising a programmable timer to indicate the predetermined interval.

7. A method, comprising:

determining, based on an address of an access to a first memory bank in an operational state, that a second memory bank in a low power state is anticipated to be subsequently accessed;

placing the second memory bank in an operational state prior to a request for said subsequent access; and

performing said subsequent access to the second memory bank.

8. The method of claim 7, wherein said determining comprises accessing an address location in the first memory bank that is within a predefined number of address locations from an address location in the second memory bank.

9. The method of claim 8, wherein said accessing comprises a processor performing a request for a memory access in the first memory bank.

10. The method of claim 8, wherein said accessing comprises a direct memory access controller performing a request for a memory access in the first memory bank.

11. The method of claim 7, further comprising placing the second memory bank in a low power state resultant to the second memory bank not being accessed for a predefined interval.

12. A system, comprising:

a processor;

a first memory bank coupled to the processor;

a second memory bank coupled to the processor and capable of having a low power state and an operational state; and

a circuit to place the second memory bank in the operational state from the low power state, responsive to the first memory bank being accessed at an address that is within a predetermined number of address locations from an address in the second memory bank.

13. The system of claim 12, wherein the circuit comprises a programmable storage element to store the address that is within the predetermined number of address locations from the address in the second memory bank.

14. The system of claim 12, wherein the first and second memory banks comprise volatile memory.

15. The system of claim 12, further comprising a programmable timer to be restarted responsive to the second memory bank being accessed.

16. The system of claim 15, wherein the circuit is to place the second memory bank into the low power state from the operational state, responsive to the timer expiring.

17. An article comprising

a machine-readable medium that provides instructions, which when executed by a processing platform, cause said processing platform to perform operations comprising:

developing code for execution, the code to extend between first and second memory bands during said execution; and

determining a threshold address for the first memory bank, the threshold address to be used to indicate that access to the first memory bank at an address above the threshold address during said code execution is to indicate that access to the second memory bank is anticipated to occur within a predetermined interval.

18. The article of claim 17, wherein said determining is based on:

an estimated time for the second memory bank to transition from a low power state to an operational state; and

an estimated time for said code execution to result in access to the second memory bank after accessing the threshold address.

19. The article of claim 17, further comprising placing instructions into the code that, when executed, will cause the second memory bank to go into an operational state.